	V1.0
	20210621

APT32S003 COUNTA

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3.1 COUNTA

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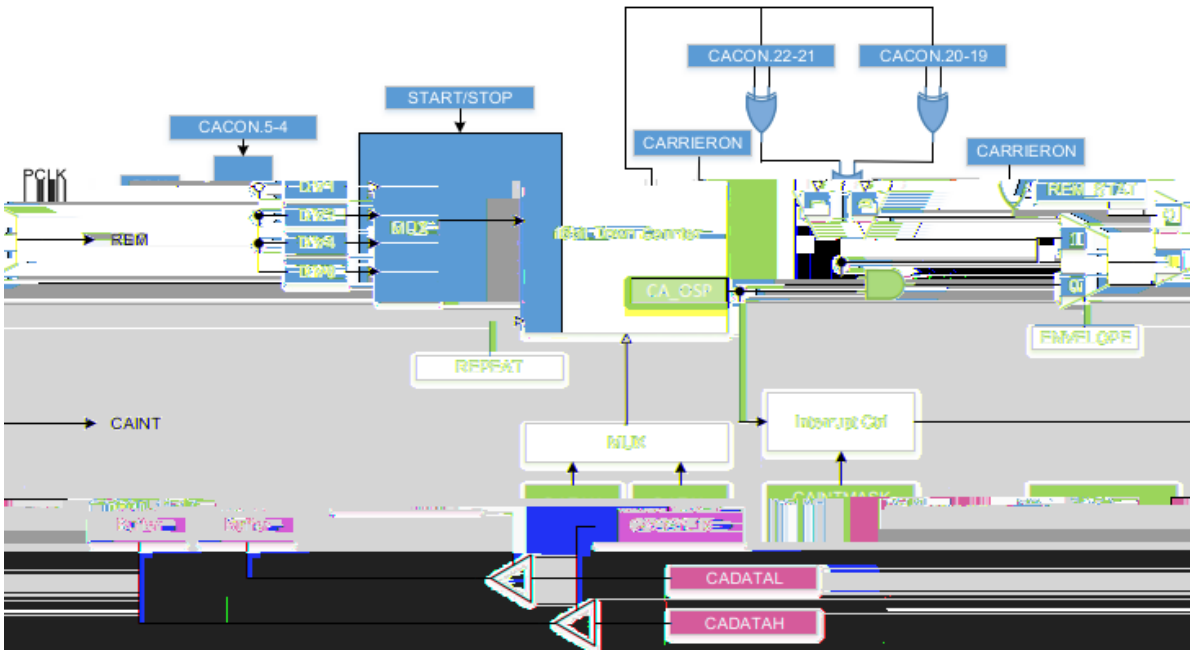

```
/*************************************************************/
//COUNTA Initial
//EntryParameter:NONE
//ReturnValue:NONE
/*************************************************************/
void COUNTA_CONFIG(void)
{
    COUNT_DeInit();                                                          //clear all countA Register
    COUNTA_IO_Init(COUNTA_PB01);                                             //set PB0.01 as counter IO
    COUNTA_Init(24000,24000,Period_H,DIV1,REPEAT_MODE,CARRIER_ON,OSP_LOW);   //Data_H=Time/(1/sysclock)
    COUNTA_Config(SW_STROBE,PENDREM_OFF,MATCHREM_OFF,REMSTAT_0,ENVELOPE_0);   //countA mode set
    COUNTA_Start();                                                          //countA start
    //COUNTA_Stop();                                                         //countA stop
    COUNTA_Int_Enable();                                                     //countA INT enable
}
```

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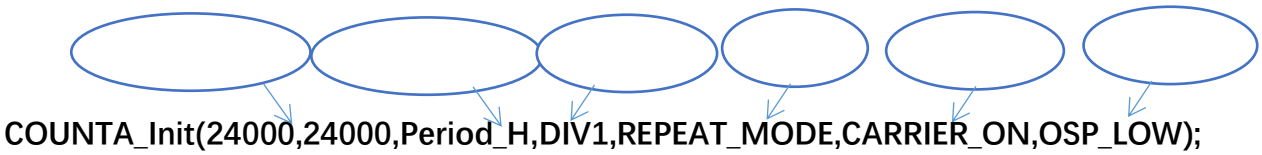

COUNTA_Init(24000,24000,Period_H,DIV1,REPEAT_MODE,CARRIER_ON,OSP_LOW);

COUNTA_Config(SW_STROBE,PENDREM_OFF,MATCHREM_OFF,REMSTAT_0,ENVELOPE_0);

3.2

```
/*************************************************************/
//COUNTA Initial
//EntryParameter:NONE
//ReturnValue:NONE
/*************************************************************/
void COUNTA_CONFIG(void)
{
    COUNT_DeInit();                                    //clear all countA Register
    COUNTA_IO_Init(COUNTA_PB01);                       //set PB0.01 as counter IO
    COUNTA_Init(24000,24000,Peri
```

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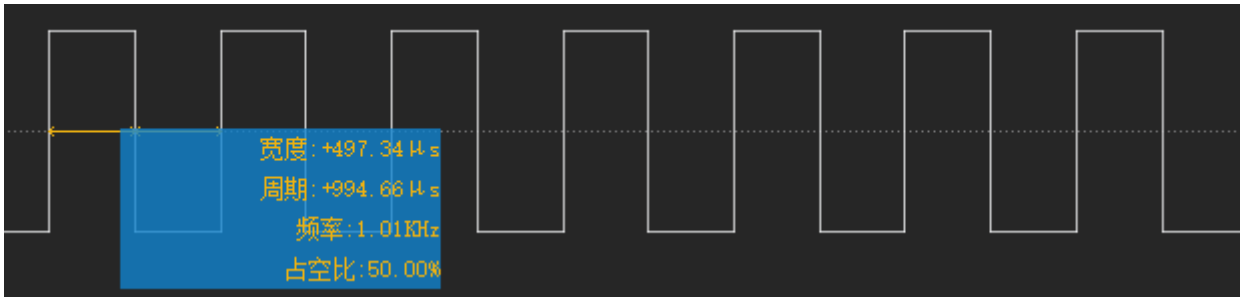

3.3

```
void GPIO_CONFIG(void)
{
    GPIO_Init(GPIOA0,10,0);
    GPIO_Write_High(GPIOA0,10);
}
/*****************************************************************/
//COUNTA Initial
//EntryParameter:NONE
//ReturnValue:NONE
/*****************************************************************/
void COUNTA_CONFIG(void)
{
    COUNT_DeInit();                                                          //clear all countA Register
    COUNTA_Init(24000,0,Period_H,DIV1,REPEAT_MODE,CARRIER_ON,OSP_LOW);       //Data_H=Time/(1/sysclock)
    COUNTA_Config(SW_STROBE,PENDREM_OFF,MATCHREM_OFF,REMSTAT_0,ENVELOPE_0);  //countA mode set
    COUNTA_Start();                                                          //countA start
    //COUNTA_Stop();                                                         //countA stop
    COUNTA_Int_Enable();                                                     //countA INT enable
}
void APT32S003_init(void)
{
//-------------------------------------------------------------/
//Peripheral clock enable and disable
//EntryParameter:NONE
//ReturnValue:NONE
//-------------------------------------------------------------/
```

```
    SYSCON->PCER0=0xFFFFFFF;                                    //PCLK Enable    0x00410071
    SYSCON->PCER1=0xFFFFFFF;                                    //PCLK Enable
    while(!(SYSCON->PCSR0&0x1));                                //Wait PCLK enabled
//-------------------------------------------------------------/
//ISOSC/IMOSC/EMOSC/SYSCLK/IWDT/LVD/EM_CMFAIL/EM_CMRCV/CMD_ERR OSC stable interrupt
//EntryParameter:NONE
//ReturnValue:NONE
//-------------------------------------------------------------/
    SYSCON_CONFIG();                                            //syscon    initial
    CK_CPU_EnAllNormalIrq();                                    //enable all IRQ
//-------------------------------------------------------------/
//Other IP config
//-------------------------------------------------------------/
   GPIO_CONFIG();
   COUNTA_CONFIG();                                             //CountA initial
}
/*****************************************************************/
//CONTA Interrupt
//EntryParameter:NONE
//ReturnValue:NONE
/*****************************************************************/
volatile U8_T f_io_toggle;
void CNTAIntHandler(void)
{
    // ISR content ...
   if(!f_io_toggle)
   {
        f_io_toggle = 1;
        GPIO_Set_Value(GPIOA0,10,1);
   }
   else
   {
        f_io_toggle=0;
        GPIO_Set_Value(GPIOA0,10,0);
   }
}
```

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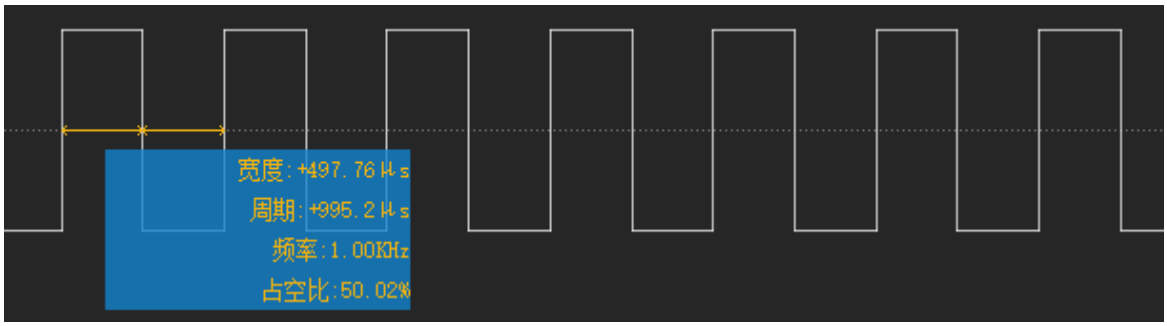

3.4

```
/*************************************************************/
//COUNTA Initial
//EntryParameter:NONE
//ReturnValue:NONE
/*************************************************************/
void COUNTA_CONFIG(void)
{       //174*48,87*48
    COUNT_DeInit();                                                         //clear all countA Register
    COUNTA_IO_Init(COUNTA_PB01);                                            //set PB0.01 as counter IO
    COUNTA_Init(8*48,18*48,Period_NA,DIV1,REPEAT_MODE,CARRIER_ON,OSP_LOW);          //Data_H=Time/(1/sysclock)
    COUNTA_Config(HW_STROBE_1,PENDREM_2,MATCHREM_1,REMSTAT_0,ENVELOPE_0);   //countA mode set
    COUNTA_Start();                                                         //countA start
    //COUNTA_Stop();                                                        //countA stop
    //COUNTA_Int_Enable();                                                  //countA INT enable
}
/*************************************************************/
//BT Initial
//EntryParameter:NONE
//ReturnValue:NONE
/*************************************************************/
void BT_CONFIG(void)
{
        BT_DeInit(BT0);
        //BT_IO_Init(BT0_PB02);
        BT_Configure(BT0,BTCLK_EN,47,BT_IMMEDIATE,BT_CONTINUOUS,BT_PCLKDIV);//TCLK=PCLK/(0+1)
        BT_ControlSet_Configure(BT0,BT_START_HIGH,BT_IDLE_LOW,BT_SYNC_DIS,BT_SYNCMD_DIS,BT_OSTMDX_ONCE,BT_AREARM_DIS,BT_CNTRL
D_EN);
        //BT_ControlSet_Configure(BT0,BT_START_HIGH,BT_IDLE_LOW,BT_SYNC_EN,BT_SYNCMD_DIS,BT_OSTMDX_ONCE,BT_AREARM_DIS,BT_CNTRL
```

```
D_EN);
        //BT_Trigger_Configure(BT0,BT_TRGSRC_PEND,BT_TRGOE_EN);
        BT_Period_CMP_Write(BT0,2250,560);
        BT_Start(BT0);
        BT_ConfigInterrupt_CMD(BT0,ENABLE,BT_PEND);
        BT0_INT_ENABLE();
}
void APT32S003_init(void)
{
//-------------------------------------------------------------/
//Peripheral clock enable and disable
//EntryParameter:NONE
//ReturnValue:NONE
//-------------------------------------------------------------/
        SYSCON->PCER0=0xFFFFFFFF;                                   //PCLK Enable   0x00410071
        SYSCON->PCER1=0xFFFFFFFF;                                   //PCLK Enable
        while(!(SYSCON->PCSR0&0x1));                                //Wait PCLK enabled
//-------------------------------------------------------------/
//ISOSC/IMOSC/EMOSC/SYSCLK/IWDT/LVD/EM_CMFAIL/EM_CMRCV/CMD_ERR OSC stable interrupt
//EntryParameter:NONE
//ReturnValue:NONE
//-------------------------------------------------------------/
        SYSCON_CONFIG();                                            //syscon   initial
        CK_CPU_EnAllNormalIrq();                                    //enable all I
        BT_CONFIG();                                                //BT initial
        COUNTA_CONFIG();                                            //CountA initial
}
```

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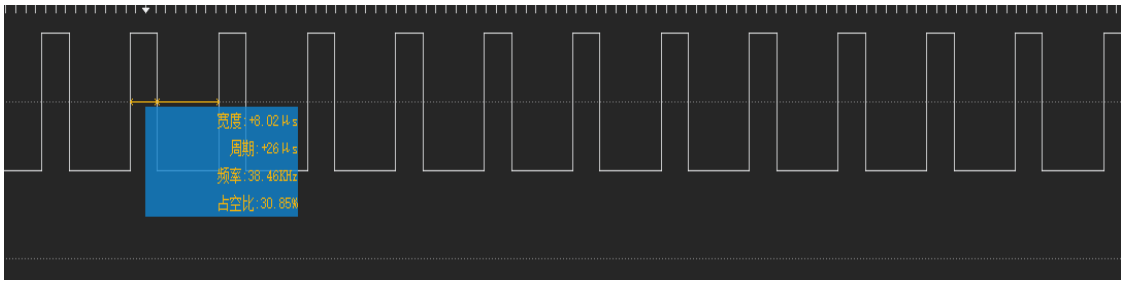

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